U.S. Patent Application Serial No. 10/639,920 Reply to Office Action Dated: August 10, 2004

## REMARKS

Favorable reconsideration of this application is requested in view of the following remarks.

Claims 1-4 and 10-13 were rejected as being anticipated by JP-10092644. The applicant traverses these rejections. The Examiner cited JP-10092644 as teaching the first and second electrodes (12,13) being insulated from each other. As can be seen in the enclosed partial translation of JP-10092644 (paragraph 18), the first and second electrodes in fact are not insulated from each other, but are connected electrically through the connecting via (14). JP-10092644 recites that "reference numeral 14 denotes a connecting via that is formed from a thick-film material such as Ag or the like and provided between the first and second internal conductor layers 12 and 13 so that the first and second internal conductor layers 12 and 13 are interconnected electrically to each other". In contrast, claim 1 of the invention recites that the first and second electrodes are insulated from each other. Claims 2-4 and 10-13 depend from claim 1. Favorable reconsideration is requested.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612)371-5237.

Respectfully submitted,

MERCHANT & GOULD P.C.

P.O. Box 2903

Minneapolis, Minnesota 55402-0903

(612) 332-5300

Dated: November 10, 2004

23552

PATENT TRADUMARK OFFICE

Douglas P. Mueller

Reg. No. 30,300

DPM:mfe

## Partial Translation of JP10(1998)-92644 A

Publication Date: April 10, 1998

Application No. :

8(1996)-242758

Filing Date:

September 13, 1996

Applicant:

Matsushita Electric Industrial Co., Ltd.

Inventors:

Minoru SOBANE

Kazuo OISHI

10

Hidekazu URYU

Title of the Invention: CHIP INDUCTOR AND METHOD OF MANUFACTURING THE SAME

15

20

25

30

35

(Page 3, left column, lines 23 – 40)

[0018] FIG. 1 is a cross-sectional view of a chip inductor according to one embodiment of the present invention. In FIG. 1, reference numeral 11 denotes a sintered magnetic body whose surface has been impregnated with siloxane having a covalent bond of aluminum. The sintered magnetic body 11 is formed by immersing pores of a porous ceramic body (not shown) in a mixed solution in which a silane coupling agent and a metal alkoxide compound are hydrolyzed and then by subjecting the hydrolysate to dehydration and condensation. Reference numerals 12 and 13 respectively denote first and second internal conductor layers that are formed from a thick-film material such as Ag or the like and provided alternately inside the sintered magnetic body 11. Further, reference numeral 14 denotes a connecting via that is formed from a thick-film material such as Ag or the like and provided between the first and second internal conductor layers 12 and 13 so that the first and second internal conductor layers 12 and 13 are interconnected electrically to each other. Reference numeral 15 denotes an external terminal electrode that is formed from a thick-film material such as Ag or the like and provided on each of opposing side faces of the sintered magnetic body 11 so as to be connected electrically to either of the first and

5

second internal conductor layers 12 and 13. Reference numerals 16 denotes a plating layer that is formed from Ni or the like and provided so as to cover the external terminal electrode 15 as required, and reference numeral 17 denotes a solder plating layer that is formed from Sn or the like and provided so as to cover the plating layer 16.